REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, captioned **"Version with markings to show changes made."**

Claims 1-9 have been canceled, without prejudice, and new claims 10-15 have been added. New claim 10 combines some, but not all, features of canceled claims 1 and 4, and claims 11-15 correspond to canceled claims 5-9, respectively.

The rejection of claims 1-9 under § 112 have been avoided in new claim 10. Withdrawal is respectfully requested.

The rejections of claims 1-10 in view of the cancellation of those claims, but the patentability of new claim 10 over the cited references will be shown.

Jung et al. '173 discloses a non-doped extended portion 240 of the semiconductor layer, storage electrode 420 connected to storage line 430, and pixel electrode 800 electrically connected to non-doped semiconductor layer 240 via drain electrode 620, doped semiconductor layer 230 and contact holes C2 and C3. A capacitor is formed between non-doped semiconductor portion 240 and storage electrode 420 via gate insulating film 300. Another capacitor is formed between storage electrode 420 and pixel electrode 800 via insulator 500 and 700.

Yamamoto et al. '071 discloses non-doped semiconductor layer 53a isolated from semiconductor layer 13, storage electrode 50B connected to storage line 50B, and pixel electrode 19 electrically connected to non-doped semiconductor layer 53a via contact electrode 50c formed in contact holes 55 and 57. A capacitor is formed between non-doped

semiconductor layer 53a and storage electrode 50b via gate insulating layer 14. Another capacitor is formed between storage electrode 50b and pixel electrode 19 via intermediate layer 18.

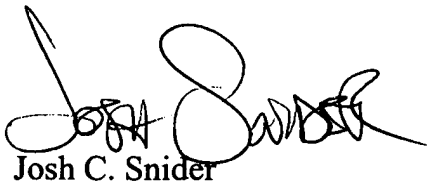
However, Jung et al. and Yamamoto et al. fail to disclose a first semiconductor layer including impurity used as a first storage capacitor electrode, a second storage capacitor electrode formed between the first and the second insulating films which are different from the gate insulating film and connected to a storage capacitor wiring maintained at a predetermined potential, wherein as least a first storage capacitor is structured by the first storage capacitor electrode including impurity, the first insulating film which is different from the gate insulating film and the second storage capacitor electrode, and a second storage capacitor structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

The storage capacitor disclose by Yamamoto et al. function as a MOS capacitor. Generally, the capacitance of MOS capacitors is changed by varying the applied voltage to the storage electrode or the characteristic of semiconductor film. To the contrary, since the storage capacitor of the present invention is not a MOS capacitor, the capacitance does not depend on the varying voltage yet is stable.

For the foregoing reasons, applicant believes that this case is in condition for allowance, which is respectfully requested. The examiner should call applicant's attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 
Josh C. Snider
Registration No. 47,954

April 29, 2002

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: 312.360.0080
Facsimile: 312.360.9315
F:\DATA\WP60\1324\63957\Amend A.doc

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

New claims 10-15 were added as follows:

10. (New) An active matrix type display comprising:

a plurality of gate wirings formed on a substrate;

a plurality of data wirings formed on the substrate substantially orthogonal to the gate wirings;

a thin film transistor formed in each of the pixel areas and structured planar type having an operating semiconductor layer formed on the substrate, a gate insulating film formed on the operating semiconductor layer, a gate electrode formed on the gate insulating film and connected to one of the gate wirings, first and second semiconductor layers formed on both sides of the operating semiconductor layer electrically connected to the pixel electrode via a contact window opened to first and second insulating layers laminated on the first semiconductor layer, and a drain electrode including the second semiconductor layer and connected to the data wirings; and

a plurality of storage capacitor electrodes using the first semiconductor layer as a first storage capacitor electrode, having a second storage capacitor electrode being formed between the first insulating film and the second insulating film and connected to a

storage capacitor wiring maintained at a predetermined potential, wherein at least a first storage capacitor is structured by the first storage capacitor electrode, the first insulating film and the second storage capacitor electrode, and a second storage capacitor is structured by the second storage capacitor electrode, the second insulating film and the pixel electrode.

11. (New) An active matrix type display as set forth in claim 10, wherein the first storage capacitor electrode uses a semiconductor layer formed isolated from the first semiconductor layer instead of the first semiconductor layer.

12. (New) An active matrix type display as set forth in claim 10, wherein a plurality of the storage capacitor electrodes have a third storage capacitor electrode formed on the first insulating film in the gate wiring area at a previous stage of the pixel area and connected to the pixel electrode in the pixel area, and a fourth storage capacitor electrode formed on the second insulating film in the gate wiring area and the data wiring area and providing an end of the pixel electrode formed on a third insulating film formed at an upper portion and an end overlapping viewing the substrate perpendicularly, wherein a third storage capacitor is structured by the third storage capacitor electrode, the second insulating film and the fourth storage capacitor electrode, and the fourth storage capacitor is structured by the fourth storage capacity electrode, the third insulating film and the pixel electrode.

13. (New) An active matrix type display as set forth in claim 12, wherein a fifth storage capacitor is structured by the third storage capacitor electrode, the first insulating film and the gate wiring.

14. (New) An active matrix type display as set forth in claim 12, wherein the fourth storage capacitor electrode also serves as a storage capacitor wiring.

15. (New) An active matrix type display as set forth in claim 12, wherein the fourth storage capacitor electrode also serves as a shading film.